## AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): A method for making an ultrathin high-k gate dielectric for use in a field effect transistor comprising:

depositing a high-k gate dielectric material on a substrate; ~~and~~

forming an ultrathin high-k dielectric by performing a thinning process on said high-k gate dielectric material, wherein the ultrathin high-k dielectric has a thickness of less than about 3 nm~~.~~; and, following the thinning process,

forming a conductive gate structure on said ultrathin high-k dielectric.

Claim 2 (Original): The method of claim 1, wherein the high-k gate dielectric material has a dielectric constant of at least about 7, and the ultrathin high-k gate dielectric has a thickness of less than about 2 nm.

Claim 3 (Original): The method of claim 2, wherein the high-k gate dielectric material has a dielectric constant ranging from about 10 to about 25, and the ultrathin high-k gate dielectric has a thickness ranging from about 1 nm to about 2 nm.

Claim 4 (Original): The method of claim 3, wherein the high-k dielectric material is selected from the group consisting of a metal oxide, a metal oxynitride, a metal silicon oxide, a metal silicon oxynitride, a metal germanium oxide, a metal germanium oxynitride, and alloys, mixtures, or multilayers of the same; wherein the metal is selected from the group consisting of Al, Ba, Be, Bi, C, Ca, Ce, Co, Cr, Dy, Eu, Fe, Ga, Gd, Hf, In, La, Li, Mg, Mn, Mo, Nb, Ni, Pr, Sc, Sr, Ta, Ti, V, W, Y, Zn, and Zr.

Claim 5 (Original): The method of claim 4, wherein the high-k dielectric material comprises $HfO_2$.

Claim 6 (Original): The method of claim 4, further comprising depositing at least one interfacial layer of a metal-free dielectric material between the substrate and the high-k gate dielectric.

Claim 7 (Original): The method of claim 6, wherein the metal-free dielectric material is selected from the group consisting of silicon oxide, germanium oxide, silicon oxynitride, germanium oxynitride, silicon nitride, and germanium nitride.

Claim 8 (Original): The method of claim 1, wherein the thinning process is selected from the group consisting of wet etching, dry etching, and hybrid damage/wet etching.

Claim 9 (Original): The method of claim 8, wherein the dry etching process is selected from the group consisting of physical sputtering, ion beam etching, reactive ion etching, and gas cluster ion beam (GCIB) processing.

Claim 10 (Original): The method of claim 8, wherein the thinning process comprises hybrid damage/wet etching treatment.

Claim 11 (Original): The method of claim 10, wherein the hybrid damage/wet etching treatment comprises an argon reactive ion etch as the damage treatment.

Claim 12 (Original): The method of claim 1, further comprising a post-thinning treatment of the high-k dielectric material.

Claim 13 (Original): The method of claim 12, wherein the post-thinning treatment is selected from the group consisting of annealing in an inert ambient, annealing in a reactive ambient, and treating with plasma.

Claim 14 (Original): The method of claim 1, further comprising adding additional material to the gate dielectric during or after the thinning, wherein the additional material is selected from the group consisting of Al, B, Ba, Be, Bi, Br, C, Ca, Ce, Cl, Co, Cr, Dy, Eu, F, Fe, Ga, Gd, Ge, H, Hf, In, La, Li, Mg, Mn, Mo, N, Nb, Ni, O, P, Pr, S, Sc, Si, Sn, Sr, Ta, Ti, V, W, Y, Zn, and Zr.

Claim 15 (Original): The method of claim 14, wherein the additional material comprises N.

Claim 16 (Original): The method of claim 1, further comprising annealing said high-k dielectric material prior to performing said thinning process.

Claim 17 (Withdrawn): An ultrathin high-k gate dielectric for use in a field-effect transistor made by a method comprising:

depositing a high-k gate dielectric material on a substrate; and

forming an ultrathin high-k dielectric by performing a thinning process on said high-k gate dielectric material, wherein the ultrathin high-k dielectric has a thickness of less than about 3 nm.

Claim 18 (Withdrawn): The gate dielectric of claim 17, wherein the high-k gate dielectric material has a dielectric constant of at least about 7, and the ultrathin high-k gate dielectric has a thickness of less than about 2 nm.

Claim 19 (Withdrawn): The gate dielectric of claim 18, wherein the high-k gate dielectric material has a dielectric constant ranging from about 10 to about 25, and the ultrathin high-k gate dielectric has a thickness ranging from about 1 nm to about 2 nm.

Claim 20 (Withdrawn): The gate dielectric of claim 19, wherein the high-k dielectric material is selected from the group consisting of a metal oxide, a metal oxynitride, a metal silicon oxide, a metal silicon oxynitride, a metal germanium oxide, a metal

germanium oxynitride, and alloys, mixtures, or multilayers of the same; wherein the metal is selected from the group consisting of Al, Ba, Be, Bi, C, Ca, Ce, Co, Cr, Dy, Eu, Fe, Ga, Gd, Hf, In, La, Li, Mg, Mn, Mo, Nb, Ni, Pr, Sc, Sr, Ta, Ti, V, W, Y, Zn, and Zr.

Claim 21 (Withdrawn): The gate dielectric of claim 20, wherein the high-k dielectric material comprises $HfO_2$.

Claim 22 (Withdrawn): The gate dielectric of claim 20, wherein the method to make said dielectric further comprises deposition at least one interfacial layer of a metal-free dielectric material between the substrate and the high-k gate dielectric.

Claim 23 (Withdrawn): The gate dielectric of claim 22, wherein the metal-free dielectric material is selected from the group consisting of silicon oxide, silicon oxynitride, and silicon nitride.

Claim 24 (Withdrawn): The gate dielectric of claim 17, wherein the thinning process is selected from the group consisting of wet etching, dry etching, and hybrid damage/wet etching.

Claim 25 (Withdrawn): The gate dielectric of claim 24, wherein the dry etching process is selected from the group consisting of physical sputtering, ion beam etching, reactive ion etching, and gas cluster ion beam (GCIB) processing.

Claim 26 (Withdrawn): The gate dielectric of claim 24, wherein the thinning process comprises hybrid damage/wet etching treatment.

Claim 27 (Withdrawn): The gate dielectric of claim 26, wherein the hybrid damage/wet etching treatment comprises an argon reactive ion etch as the damage treatment.

Claim 28 (Withdrawn): The gate dielectric of claim 17, wherein the method to make said dielectric further comprises a post-thinning treatment of the high-k dielectric material.

Claim 29 (Withdrawn): The gate dielectric of claim 28, wherein the post-thinning treatment is selected from the group consisting of annealing in an inert ambient, annealing in a reactive ambient, and treating with plasma.

Claim 30 (Withdrawn): The gate dielectric of claim 17, further comprising adding additional material to the gate dielectric during or after the thinning, wherein the additional material is selected from the group consisting of Al, B, Ba, Be, Bi, Br, C, Ca, Ce, Cl, Co, Cr, Dy, Eu, F, Fe, Ga, Gd, Ge, H, Hf, In, La, Li, Mg, Mn, Mo, N, Nb, Ni, O, P, Pr, S, Sc, Si, Sn, Sr, Ta, Ti, V, W, Y, Zn, and Zr.

Claim 31 (Withdrawn): The gate dielectric of claim 30, wherein the additional material comprises N.

Claim 32 (Withdrawn): The gate dielectric of claim 17, wherein the method to make said dielectric further comprises annealing said high-k dielectric material prior to performing said thinning process.